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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,959	06/20/2001	Hidemasa Zama	210067US-2	2668

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EXAMINER
TAN, VIBOL

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/883,959	Applicant(s) ZAMA ET AL.	
	Examiner Vibol Tan	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-13 and 17* is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 2, 9, and 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim objections

2. Claim 3 recites the limitation "said first transistor" in line 8. There is insufficient antecedent basis for this limitation in the claim.

3. Claims 5, 8, and 11 are objected in the same manner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Bosshart (U.S. PAT. 5,821,778).

Bosshart teaches in Fig. 1 all acclaimed features of claims 1 and 2, a semiconductor integrated circuit comprising: a plurality of gate circuits (Fig. 1); and a control circuit (gated clock circuit not shown) configured to control the operation of some gate circuits (22, 24) among said plurality of gate circuits, each of said some gate

circuits among said plurality of gate circuits including: a logic circuit constituted by a plurality of first transistors (NMOS); and a switch circuit (12) which can switch whether a power supply voltage (V_{DD}) is supplied to said logic circuit, is constituted by a second transistor (PMOS) having a threshold voltage higher than that of said first transistor, and is controlled by said control circuit (gated clock), wherein said some gate circuits are provided on a critical path.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 3-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwaki et al. (U.S. PAT. 6,208,170).

Iwaki et al. teaches all claimed features of claims 3 and 4 in Fig. 4, a logic operation circuit comprising: a gate circuit (301) which is connected between a virtual voltage line (QVCC) and a first reference voltage line (VSS) and constituted by a plurality of first transistors (112,113); and a second transistor (104) which is connected between a second reference voltage line (VCC) and said virtual voltage line and constituted by a transistor having a threshold voltage higher (col. 4, line 28) than that of said first transistor, a source/drain terminal of said first transistor in said gate circuit

being connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal (output from 301) of said gate circuit, wherein said logic operation circuit defined in claim 3 is provided on a critical path.

Regarding claims 5-7, Iwaki et al. teaches all claimed features in Fig. 7, a logic operation circuit comprising: a gate circuit (101) which is connected between a first reference voltage line (VCC) and a virtual voltage line (QVSS) and constituted by a plurality of first transistors (112, 113); a second transistor (205) which is connected between said virtual voltage line and a second reference voltage line (VSS) and has a threshold voltage higher (col. 7, line 26) than that of said first transistor; and a third transistor (204) which is connected between said first reference voltage line and an output terminal (via 112) of said gate circuit and has a threshold voltage higher (col. 7, line 25) than that of said first transistor, said second and third transistors being on/off-controlled in such a manner that one of them is turned on while the other is turned off and vice versa, wherein a source/drain terminal of said first transistor in said gate circuit is connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal (from 101), of said gate circuit wherein said logic operation circuit defined in claim 5 is provided on a critical path.

In claims 8-10, Iwaki et al. teaches all claimed features in Fig. 2, a logic operation circuit comprising: a gate circuit (301) which is constituted by a plurality of first transistors (312-313) and connected to first and second virtual voltage lines (QVCC, QVSS); a second transistor (304) which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher (col. 2, line 15)

than said first transistor; a third transistor (305) which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher (col. 2, line 15) than that of said first transistor; and a storage circuit (303) capable of holding output logic of said gate circuit, said second and third transistors being controlled to be OFF when said storage circuit holds said output logic of said gate circuit, and said second and third transistors being controlled to be ON when said storage circuit does not hold said output logic of said gate circuit, wherein a source/drain terminal of said first transistor in said gate circuit is connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit, wherein said logic operation circuit is provided on a critical path.

8. Claims 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 11-13 and 17 are allowed.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bosshart teaches data storage circuits using low threshold voltage output enable circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

Vibol Tan

Patent Examiner, AU 2819

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800